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LAMINATED TYPE SEMICONDUCTOR PACAKGE

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[There are no amendments to this patent.]

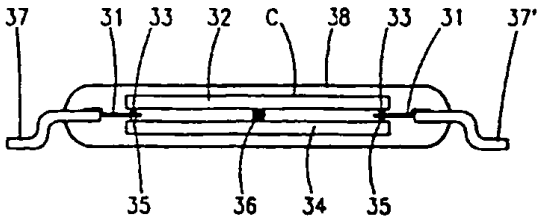
Abstract

Objective

To provide a laminated semiconductor package which can make the semiconductor package ultrathin by utilizing TAB technology and C-4 bonding technology.

Constitution

A laminated semiconductor package is constituted in which a chip set is formed by solder bumps of the top and bottom side bare chips adhered to both side surfaces of the inner lead of a TAB tape; said top and bottom side bare chips are joined with solder, and the bare chips are laminated by the out lead of the TAB tape of said chip set adhered to the lead frame. Laminated chip set is composed by a lead frame inserted and adhered between two bare chips, and the design is very simple.



Claims

1. A laminated smeicondutor package composed by solder bumps (33) and (35) of top and bottom side bare chips (32) and (34) adhered to both side surfaces of the inner lead of TAB tape (31), chip set (C) being formed by said top and bottom side bare chips (32) and (34) being joined with solder (36), the output lead of TAB tape (31) adhered to said chip set (C) being adhered to lead frames (37) and (37'), and two bare chips (32) and (34) being laminated.

2. A laminated semiconductor package composed by solder bumps (33) and (35) of top and bottom side bare chips (32) and (34) adhered to both side surfaces of the inner lead of top side TAB tape (31), top and botomm side bare chips (32) and (34) joined with solder (36), solder bumps (43) and (45) of top and bottom side bare chips (42) and (44) being adhered to both side surfaces of the inner lead of bottom side TAB tape (41), said top and bottom side bare chips (42) and (44) being joined with solder (46), each out lead of said top and bottom side TAB tapes (31) and (41) adhered to the top and bottom side surfaces of lead frames (47) and (47'), and four bare chips (32), (34), (42) and (44) being laminated.

3. A laminated semiconductor package noted in Claim 2, composed by adhesive (51) being coated between inside bare chips (34) and (42).

4. A laminated semiconductor package noted in Claim 1 or 2, composed by the out leads of said TAB tapes (31) and (41) being respectively adhered to SOJ lead frames (47) and (47').

5. A laminated semiconductor package noted in Claim 1 or 2, composed by the out leads of said TAB tapes (31) and (41) being respectively adhered to baddo [transliteration] lead frames (48) and (48').

6. A laminated semiconductor package noted in Claim 1 or 2, composed by the out leads of said TAB tapes (31) and (41) being respectively adhered to SOP lead frames (49) and (49').

7. A laminated semiconductor package composed by laminated type chip set (C) formed by lead frames (37) and (37') being inserted and adhered by just a prescribed length between top and bottom side bare chips (32) and (34), TAB tapes (31) and (31) being adhered to one side ends of said lead frames (37) and (37'), and the leads of said TAB tapes (31) and (31) being adhered to solder bumps (33) and (35) formed at the pad part of said top and bottom side bare chips (32) and (34), and said chip set (C) being mold encapsulated so that the other side ends of said lead frames (37) and (37') are exposed.

8. A laminated semiconductor package noted in Claim 7, which is composed by the length of said lead frames (37) and (37') inserted in top and bottom side bare chips (32) and (34) being varied according to the pad position of said top and bottom side bare chips (32) and (34).

9. A laminated semiconductor package noted in Claim 7, in which said chip set (C) is composed of chip set (C) laminated

with a plurality of chip sets, and after the other side ends of the lead frames of the chip sets in said chip set (C) are coupled as one body by respectively projecting to the left and right sides, said chip set (C) is mold encapsulated so that it is molded into one body again and the left and right side lead frames of chip set (C) are exposed from the coupled part.

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